A1 (cont'd)

8. (Amended) The EDS protection circuit as claimed in claim 6, wherein the gate is applied with a bias voltage to speed up the turn-on rate of the substrate-triggered MOS when an ESD event occurs.

A2

13. (Amended) The ESD protection circuit as claimed in claim 1, wherein the diode includes a PN junction diode formed by a PN junction between a first source/drain and a substrate of a MOS.

A3

15. The ESD protection circuit as claimed in claim 13, wherein the gate of said MOS is coupled to a second source/drain of the MOS.